SPECIFICATION AMENDMENTS

Please replace paragraph 0017 with the following rewritten paragraph:

Fig. 2 first shows the results of thermally annealing the microelectronic product of Fig.1 to form from the blanket metal silicide forming metal layer 16 and the blanket undoped silicon layer 16 18 (if present) a blanket metal silicide layer 17. Since the blanket metal silicide forming metal layer 16 is formed upon the blanket barrier layer 14, the thermal annealing proceeds such that a doped polysilicon layer is neither formed nor remains interposed between the blanket metal silicide layer 17 and the blanket barrier layer 14 or the contact region 12. Such thermal annealing also partially (and minimally) consumes the blanket first doped polysilicon layer 20 to form a partially consumed blanket first doped polysilicon layer 20'. When the blanket undoped silicon layer 18 is absent, the blanket metal silicide layer 17 is formed in conjunction with an enhanced consumption of the blanket first doped polysilicon layer 20. The use of the optional blanket undoped silicon layer 18 is desirable since the same provides for limited doping of the blanket metal silicide layer 17. The thermal annealing is undertaken at a temperature and for a time period appropriate for a metal silicide forming metal from which is formed the blanket metal silicide forming metal layer 16. Typically, the thermal annealing is undertaken at a temperature of from about 900 to about 1100 degrees

centigrade and a rapid thermal annealing (i.e., thermal annealing temperature rise of from about 0.5 to about 2.0 seconds) time period of from about 0.5 to about 2.0 minutes, particularly when the blanket metal silicide forming metal layer 16 is formed of a titanium metal silicide forming metal.

Please replace paragraph 0033 with the following rewritten paragraph:

The blanket anti-fuse material layer may be formed of anti-fuse materials as are conventional in the microelectronic product fabrication art. Such anti-fuse materials may include, but are not limited to amorphous silicon or amorphous carbon anti-fuse materials, as well as more conventional dielectric anti-fuse materials, such as but not limited to silicon oxide, silicon nitride and silicon oxynitride dielectric anti-fuse materials. Preferably, the blanket anti-fuse material layer 24 is formed at least in part of a silicon oxide anti-fuse material, formed to a thickness of from about 10 to about 50 angstroms.

Please replace paragraph 0034 with the following rewritten paragraph:

Fig. 4 also shows a patterned second doped polysilicon layer 26 formed upon the blanket anti-fuse material layer 24 and nominally centered above the patterned first doped polysilicon layer 20a. The pair of patterned planarized second dielectric layers 28a and 28b adjoining a pair of sidewalls of the patterned

second doped polysilicon layer 26 may be formed of materials and in a manner explained above with respect to the pair of patterned planarized first dielectric layers. Analogously with the patterned first doped polysilicon layer 20a, the patterned second doped polysilicon layer 26 may also be formed of either dopant polarity (i.e., N or P) or either dopant concentration (i.e., - or +). The present invention provides particular value, however, under circumstances where the patterned second doped polysilicon layer 26 is formed of an N polarity and a - dopant concentration (i.e., from about 1E15 to about 1E17 dopant atoms per cubic centimeter) under circumstances where the patterned first doped polysilicon layer ~~24a~~ 20a is formed of a P+ polarity (or an analogous bilateral complementary dopant polarity and concentration ordering). Under such circumstances, an anti-fuse structure of the invention when fused provides a diode conductor structure rather than a pure conductor structure.